

AMENDMENTS TO THE CLAIMS

(IN REVISED FORMAT COMPLIANT WITH THE PROPOSED

REVISION TO 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus comprising:

A3  
Sub B3  
5 a first ~~delay~~ circuit configured to (i) receive a data  
signal having a first setup/hold window with respect to a clock  
signal and (ii) present a data delayed data signal having a second  
setup/hold window with respect to said clock signal, wherein (i) a  
difference between said first setup/hold window and said second  
setup/hold window is configured in response to one or more of a  
plurality of delay times, wherein (ii) each of said plurality of  
delay times is less than a period of said clock signal and (iii)  
10 said plurality of delay times provide provides a user configurable  
delay of said second setup/hold time window relative to a  
transition of said clock signal.

2. (ORIGINAL) The apparatus according to claim 1,  
further comprising:

a second circuit configured to receive said data delayed  
signal and present a data output.

3. (CURRENTLY AMENDED) The apparatus according to claim 2, wherein said second circuit comprises a register that is further configured in response to a said clock signal.

A3  
Sub B3  
4. (ORIGINAL) The apparatus according to claim 1, wherein said first delay circuit further comprises an HSTL circuit configured to present a first signal in response to a data input.

5. (ORIGINAL) The apparatus according to claim 4, wherein said first delay circuit further comprises one or more delay circuits each configured to present an output delay signal in response to said first signal.

6. (ORIGINAL) The apparatus according to claim 5, wherein said first delay circuit further comprises a switch configured to receive said one or more output delay signals and present said data delayed signal.

7. (ORIGINAL) The apparatus according to claim 6, wherein said switch is further configured in response to a user configuration signal.

8. (ORIGINAL) The apparatus according to claim 7, wherein said user configuration signal comprises a setup and hold timing configuration signal.

A3  
Sub B3  
9. (ORIGINAL) The apparatus according to claim 7, wherein said user configuration signal comprises a programmable signal.

10. (ORIGINAL) The apparatus according to claim 7, wherein said user configuration signal comprises a multi-bit signal.

11. (CURRENTLY AMENDED) An apparatus comprising:  
means for receiving ~~an input~~ a data signal having a first setup/hold window with respect to a clock signal; and

5 means for presenting a ~~data~~ delayed data signal having a second setup/hold window with respect to said clock signal, wherein  
(i) a difference between said first setup/hold window and said second setup/hold window is configured in response to one or more  
of a plurality of delay times, ~~one of a~~ (ii) each of said plurality  
of delay times is less than a period of said clock signal and (iii)  
10 said plurality of delay times ~~to provide~~ provides a user  
configurable delay of said second setup/hold time window relative  
to a transition of said clock signal.

12. (CURRENTLY AMENDED) A method for programming a data delayed signal, comprising the steps of:

(A) receiving ~~an input~~ a data signal having a first setup/hold window with respect to a clock signal; and

5 (B) configuring ~~said data~~ a delayed data signal having a second setup/hold window with respect to said clock signal, wherein (i) a difference between said first setup/hold window and said second setup/hold window is configured in response to one or more of a plurality of delay times, (ii) each of said plurality of  
10 delay times is less than a period of said clock signal and (iii) said plurality of delay times to provide provides a user configurable delay of said second setup/hold time window relative to a transition of a clock signal.

13. (ORIGINAL) The method according to claim 12, further comprising the steps of:

(C) storing said data delayed signal and presenting a data output signal.

14. (CANCELLED)

15. (ORIGINAL) The method according to claim 12, wherein step (B) further comprises presenting a first signal in response to said input signal.

A3  
Sub B3  
16. (ORIGINAL) The method according to claim 15, wherein step (B) further comprises presenting one or more output delay signals in response to said first signal.

17. (ORIGINAL) The method according to claim 16, wherein step (B) further comprises receiving said one or more output delay signals and presenting said data delayed signal.

18. (ORIGINAL) The method according to claim 17, wherein step (B) further comprises switching said one or more output delays in response to a user configuration signal.

19. (ORIGINAL) The method according to claim 18, wherein said user configuration signal comprises either (i) a setup and hold timing configuration signal or (ii) a multi-bit signal.

20. (ORIGINAL) The method according to claim 18, wherein said user configuration signal comprises a programmable signal.

App Sub B3

21. (NEW) The apparatus according to claim 1, wherein a total of all of said plurality of delay times is less than said period of said clock.